AMENDMENTS TO CLAIMS

1. (original) An active pixel sensor, comprising:

a plurality of pixels, wherein each of said pixels comprises:

a reset portion for resetting a photosensitive element of said pixel;

a first storage node for storing a reset voltage level of said photosensitive element; and

a second storage node for storing a voltage level of said photosensitive element after an integration period.

2. (original) The active pixel sensor of claim 1, wherein said photosensitive element is a photodiode.

3. (original) The active pixel sensor of claim 1, wherein each of said pixels further comprises:

a column bus coupled to said first storage node and said second storage node for receiving said reset voltage level and said voltage level of said photosensitive element after integration.

4. (original) The active pixel sensor of claim 3, wherein said first storage node further comprises a first sample and hold circuit.

5. (original) The active pixel sensor of claim 4, wherein said first sample and hold circuit comprises:

a first sample and hold transistor switchably coupling a first terminal of a first storage capacitor with said reset portion.

6. (original) The active pixel sensor of claim 5, wherein said first terminal of said first storage capacitor is coupled to a gate of a first source follower transistor, a first source/drain terminal of said first source follower transistor is coupled to a supply voltage terminal, and a second source/drain terminal of said first source follower transistor is switchably coupled to said column bus.

7. (original) The active pixel sensor of claim 6, wherein said second storage node comprises a second sample and hold circuit.

8. (original) The active pixel sensor of claim 7, wherein said second sample and hold circuit comprises:

a second sample and hold transistor switchably coupling a first terminal of a second storage capacitor with said reset portion.

9. (original) The active pixel sensor of claim 7, wherein said first terminal of said second storage capacitor is coupled to a gate of a second source follower transistor, a first source/drain terminal of said second source follower transistor is coupled to a supply voltage terminal, and a second source/drain terminal of said second source follower transistor is switchably coupled to said column bus.

10. (original) An active pixel sensor, comprising:

a plurality of pixels, wherein each of said pixels comprises:

a reset portion for resetting a photosensitive element of said pixel; and

a capacitor coupled between a clamp switch and a first source follower transistor of said reset portion, said capacitor being configured to store a reset voltage of said photosensitive element.

11. (original) The active pixel sensor of claim 10, wherein each of said pixels further comprises:

a column bus coupled to said storage node for receiving said reset voltage level.

12. (original) The active pixel sensor of claim 11, wherein each of said pixels further comprises:

a gate of a second source follower transistor coupled to said capacitor and said clamp switch, said second source follower transistor switchably coupling said capacitor to said column bus.

13. (original) The active pixel sensor of claim 12, wherein each of said pixels further comprises:

a first source/drain terminal of a load transistor coupled to ground; and

a second source/drain terminal of said load transistor coupled to said first source follower transistor and said storage capacitor.

14. (original) The active pixel sensor of claim 13, wherein each of said pixels further comprises:

a selection transistor coupled between said load transistor and ground for controlling selection of said reset portion.

15. (original) The active pixel sensor of claim 12, wherein each of said pixels further comprises:

a switch switchably coupling said first source follower transistor and said clamp capacitor to a second column bus for separately reading out said reset voltage.

16. (original) The active pixel sensor of claim 10, wherein each of said pixels further comprises:

a cascaded integration portion within said reset portion for increasing dynamic range of said pixel.

17. (original) A semiconductor chip, comprising:

an active pixel sensor, said active pixel sensor comprising:

a plurality of pixels, wherein each of said pixels comprises:

a reset portion for resetting a photosensitive element of said pixel;

a first storage node for storing a reset voltage level of said photosensitive element; and

a second storage node for storing a voltage level of said photosensitive element after an integration period.

18. (original) The semiconductor chip of claim 17, wherein said photosensitive element is a photodiode.

19. (original) The semiconductor chip of claim 17, wherein each of said pixels further comprises:

a column bus coupled to said first storage node and said second storage node for receiving said reset voltage level and said voltage level of said photosensitive element after integration.

20. (original) The semiconductor chip of claim 19, wherein said first storage node further comprises a first sample and hold circuit.

21. (original) The semiconductor chip of claim 20, wherein said first sample and hold circuit comprises:

a first sample and hold transistor switchably coupling a first terminal of a first storage capacitor with said reset portion.

22. (original) The semiconductor chip of claim 21, wherein said first terminal of said first storage capacitor is coupled to a gate of a first source follower transistor, a first source/drain terminal of said first source follower transistor is coupled to a supply voltage terminal, and a second source/drain terminal of said first source follower transistor is switchably coupled to said column bus.

23. (original) The semiconductor chip of claim 22, wherein said second storage node comprises a second sample and hold circuit.

24. (original) The semiconductor chip of claim 23, wherein said second sample and hold circuit comprises:

a second sample and hold transistor switchably coupling a first terminal of a second storage capacitor with said reset portion.

25. (original) The semiconductor chip of claim 24, wherein said first terminal of said second storage capacitor is coupled to a gate of a second source follower

transistor, a first source/drain terminal of said second source follower transistor is coupled to a supply voltage terminal, and a second source/drain terminal of said second source follower transistor is switchably coupled to said column bus.

26. (original) A semiconductor chip, comprising:

an active pixel sensor, said active pixel sensor comprising:

a plurality of pixels, wherein each of said pixels comprises:

a reset portion for resetting a photosensitive element of said pixel; and

a capacitor coupled between a clamp switch and a first source follower transistor of said reset portion, said capacitor being configured to store a reset voltage of said photosensitive element.

27. (original) The semiconductor chip of claim 26, wherein each of said pixels further comprises:

a column bus coupled to said storage node for receiving said reset voltage level.

28. (original) The semiconductor chip of claim 27, wherein each of said pixels further comprises:

a gate of a second source follower transistor coupled to said capacitor and said clamp switch, said second source follower transistor switchably coupling said capacitor to said column bus.

29. (original) The semiconductor chip of claim 28, wherein each of said pixels further comprises:

a first source/drain terminal of a load transistor coupled to ground; and

a second source/drain terminal of said load transistor coupled to said first source follower transistor and said storage capacitor.

30. (original) The semiconductor chip of claim 29, wherein each of said pixels further comprises:

a selection transistor coupled between said load transistor and ground for controlling selection of said reset portion.

31. (original) The semiconductor chip of claim 28, wherein each of said pixels further comprises:

a switch switchably coupling said first source follower transistor and said clamp capacitor to a second column bus for separately reading out said reset voltage.

32. (original) The semiconductor chip of claim 26, wherein each of said pixels further comprises:

a cascaded integration portion within said reset portion for increasing dynamic range of said pixel.

33. (original) A processor system, comprising:

a processor; and

an imager device coupled to said processor for sending signals to said processor, said imager device comprising:

a plurality of pixels, wherein each of said pixels comprises:

a reset portion for resetting a photosensitive element of said pixel;

a first storage node for storing a reset voltage level of said photosensitive element; and

a second storage node for storing a voltage level of said photosensitive element after an integration period.

34. (original) The processor system of claim 33, wherein said photosensitive element is a photodiode.

35. (original) The processor system of claim 33, wherein each of said pixels further comprises:

a column bus coupled to said first storage node and said second storage node for receiving said reset voltage level and said voltage level of said photosensitive element after integration.

36. (original) The processor system of claim 35, wherein said first storage node further comprises a first sample and hold circuit.

37. (original) The processor system of claim 36, wherein said first sample and hold circuit comprises:

a first sample and hold transistor switchably coupling a first terminal of a first storage capacitor with said reset portion.

38. (original) The processor system of claim 37, wherein said first terminal of said first storage capacitor is coupled to a gate of a first source follower transistor, a first source/drain terminal of said first source follower transistor is coupled to a supply voltage terminal, and a second source/drain terminal of said first source follower transistor is switchably coupled to said column bus.

39. (original) The processor system of claim 38, wherein said second storage node comprises a second sample and hold circuit.

40. (original) The processor system of claim 39, wherein said second sample and hold circuit comprises:

a second sample and hold transistor switchably coupling a first terminal of a second storage capacitor with said reset portion.

41. (original) The processor system of claim 40, wherein said first terminal of said second storage capacitor is coupled to a gate of a second source follower transistor, a first source/drain terminal of said second source follower transistor is coupled to a supply voltage terminal, and a second source/drain terminal of said second source follower transistor is switchably coupled to said column bus.

42. (original) A processor system, comprising:

a processor; and

an imager device coupled to said processor for sending signals to said processor, said imager device comprising:

a plurality of pixels, wherein each of said pixels comprises:

a reset portion for resetting a photosensitive element of said pixel; and

a capacitor coupled between a clamp switch and a first source follower transistor of said reset portion, said capacitor being configured to store a reset voltage of said photosensitive element.

43. (original) The processor system of claim 42, wherein each of said pixels further comprises:

a column bus coupled to said storage node for receiving said reset voltage level.

44. (original) The processor system of claim 43, wherein each of said pixels further comprises:

a gate of a second source follower transistor coupled to said capacitor and said clamp switch, said second source follower transistor switchably coupling said capacitor to said column bus.

45. (original) The processor system of claim 44, wherein each of said pixels further comprises:

a first source/drain terminal of a load transistor coupled to ground; and

a second source/drain terminal of said load transistor coupled to said first source follower transistor and said storage capacitor.

46. (original) The processor system of claim 45, wherein each of said pixels further comprises:

a selection transistor coupled between said load transistor and ground for controlling selection of said reset portion.

47. (original) The processor system of claim 44, wherein each of said pixels further comprises:

a switch switchably coupling said first source follower transistor and said clamp capacitor to a second column bus for separately reading out said reset voltage.

48. (original) The processor system of claim 42, wherein each of said pixels further comprises:

a cascaded integration portion within said reset portion for increasing dynamic range of said pixel.

49. (original) A method for operating an active pixel sensor, the method comprising:

resetting a photosensitive element of a pixel;

storing a reset voltage of said photosensitive element within said pixel;

exposing said photosensitive element to a light source during an integration period while said reset voltage is stored within said pixel; and

storing within said pixel a voltage level of said photosensitive element after said integration period, said reset voltage still being stored within said pixel.

50. (original) The method of claim 49 further comprising:

reading out said reset voltage from said pixel;

reading out said voltage level of said photosensitive element after said integration period; and

generating a difference signal corresponding to a level of light to which said photosensitive element was exposed during said integration period.

51. (original) The method of claim 50, wherein said act of reading out said reset voltage comprises:

reading out said reset voltage on a column bus running through at least a portion of said pixel.

52. (original) The method of claim 50, wherein said act of reading out said voltage level comprises:

reading out said voltage level of said photosensitive element on a column bus running through at least a portion of said pixel.

53. (new) An active pixel sensor, comprising:

a plurality of pixels, wherein each of said pixels comprises:

at least one sample and hold circuit for storing at least one of a reset voltage and a voltage level of a photosensitive element after an integration period.